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Listing of the Claims

Please amend the claims as follows:

1. (Currently Amended) A transmission line tap circuit, comprising:

at least two input terminals configured for coupling to a transmission line;

impedance load circuitry configured to provide an impedance load to the transmission line for tapping the transmission line and receiving a transmission signal propagating there through, wherein the impedance load circuitry comprises circuitry configured to provide a dissipation load for the received transmission signal;

amplifying circuitry configured to amplify the received transmission signal and directly connected to the impedance load circuitry, wherein the impedance load circuitry configured to provide the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry;

impedance matching circuitry configured to provide an impedance match to an impedance load of at least one Line Interface Unit (LIU) and directly connected to a plurality of outputs of the amplifying circuitry; and

at least two output terminals configured for coupling said transmission signal to the at least one LIU and directly connected to the impedance matching circuitry.

2. (Currently Amended) The circuit according to Claim 1, wherein the impedance load circuitry ~~configured to provide the impedance load to the transmission line~~, the amplifying circuitry ~~configured to amplify the received transmission signal~~, and the impedance matching circuitry ~~configured to provide the impedance match to the impedance load of the at least one LIU~~ are provided within a single stage.

3. (Currently Amended) The circuit according to Claim 1, wherein the impedance load circuitry ~~configured to provide the impedance load to the transmission line~~ includes at least two resistors where a first of the at least two resistors is

connected to a first of the at least two input terminals and a second of the at least two resistors is connected to a second of the at least two input terminals.

4. (Currently Amended) The circuit according to Claim 1, wherein the impedance load circuitry further ~~comprising~~ comprises circuitry configured to block direct current present in the received transmission signal.

5. (Original) The circuit according to Claim 4, wherein the circuitry configured to block direct current includes at least a first capacitor connected to a first of the at least two input terminals and a second capacitor connected to a second of the at least two input terminals.

6. (Cancelled)

6 7. (Currently Amended) The circuit according to Claim [[6]] 1, wherein the circuitry configured to provide a dissipation load for the received transmission signal includes at least two resistors connected in series ~~and coupled to the at least two input terminals~~ to form a resistor chain, a first end of the resistor chain coupled to a first input terminal of the amplifying circuitry and a second end of the resistor chain coupled to a second input terminal of the amplifying circuitry.

7 8. (Currently Amended) The circuit according to Claim 1, wherein the impedance load circuitry further ~~comprising~~ comprises circuitry configured to suppress noise in the received transmission signal and to shape the received transmission signal.

8 9. (Original) The circuit according to Claim 7 8, wherein the circuitry configured to suppress noise in the received transmission signal and to shape the received transmission signal includes at least two capacitors connected in series and coupled to the at least two input terminals.

9 ~~10~~. (Currently Amended) The circuit according to Claim 1, wherein the amplifying circuitry ~~configured to amplify the received transmission signal~~ includes circuitry configured to wave shape the received transmission signal, at least two amplifiers each having respective feedback resistors, and at least two capacitors in parallel to a respective one of the feedback resistors.

10 ~~11~~. (Currently Amended) The circuit according to Claim 1, wherein the impedance load circuitry further ~~comprising~~ comprises circuitry configured to provide a dissipation load to the amplifying circuitry ~~configured to amplify the received transmission signal~~.

11 ~~12~~. (Currently Amended) The circuit according to Claim 10 ~~11~~, wherein the circuitry configured to provide a dissipation load is in parallel to the amplifying circuitry ~~configured to amplify the received transmission signal~~ and includes at least two resistors connected in series to form a resister chain, one end of the resistor chain coupled to one of the at least two output terminals and another end of the resistor chain coupled to another of the at least two output terminals.

12 ~~13~~. (Currently Amended) The circuit according to Claim 1, wherein the impedance matching circuitry further ~~comprising~~ comprises circuitry configured to block direct current from the amplifying circuitry ~~configured to amplify the received transmission signal~~.

13 ~~14~~. (Currently Amended) The circuit according to Claim 12 ~~13~~, wherein the circuitry configured to block direct current includes at least two capacitors, ~~connected in series and~~ a first capacitor of the at least two capacitors coupled to one of the plurality of outputs of the amplifying circuitry and one of the at least two output terminals, a second capacitor of the at least two capacitors coupled to another of the plurality of outputs of the amplifying circuitry and another of the at least two output terminals.

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~~15~~. (Original) The circuit according to Claim 1, wherein the transmission line is a T1 transmission line.

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~~16~~. (Original) The circuit according to Claim 1, wherein the transmission line is a E1 transmission line.

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~~17~~. (Currently Amended) The circuit according to Claim 1, ~~further comprising gain adjustment circuitry~~ wherein at least a portion of at least one of the impedance load circuitry, the amplifying circuitry, and the impedance matching circuitry is configured to adjust the gain of the circuit.

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~~18~~. (Currently Amended) A method for interfacing a transmission line with at least one Line Interface Unit (LIU), the method comprising the steps of:

providing an impedance load to the transmission line for tapping the transmission line and receiving, via at least two input terminals, a transmission signal propagating there through;

providing a dissipation load for the received transmission signal;

amplifying the received transmission signal via amplifying circuitry directly connected to the impedance load, wherein the dissipation load provides at least two varying voltages to at least two input terminals of the amplifying circuitry;

providing an impedance match to an impedance load of the at least one LIU via direct connection from a plurality of outputs of the amplifying circuitry; and

providing, via at least two output terminals, the amplified signal to the at least one LIU.

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~~19~~. (Currently Amended) The method according to Claim ~~18~~ 17, further comprising the steps of:

blocking direct current present in the received transmission signal;

~~providing a dissipation load for the received transmission signal;~~ and

suppressing noise in the received transmission signal.

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~~20~~. (Currently Amended) A transmission line tap circuit, comprising:

means for providing an impedance load to a transmission line for tapping the transmission line and receiving, via at least two input means, a transmission signal propagating there through, wherein the means for providing an impedance load comprises a means for providing a dissipation load for the received transmission signal;

means for amplifying the received transmission signal, ~~such~~ the means for amplifying being directly connected to the impedance load, wherein the means for providing the dissipation load provides at least two varying voltages to the means for amplifying the received transmission signal; and

means for providing an impedance match to an impedance load of at least one Line Interface Unit (LIU) for providing, via at least two output means, the amplified signal to the at least one LIU, such that the means for providing the impedance match is directly connected to a plurality of outputs of the means for amplifying.